IN THE SPECIFICATION

Please insert the following heading at page 1, before line 1:

B1 TITLE OF THE INVENTION

Please amend the title at page 1, lines 1-2, as follows:

B2 SHIFT REGISTER USING M.I.S. TRANSISTORS ~~HAVING THE SAME POLARITY~~ AND SUPPLEMENTARY COLUMN

Please insert the following paragraph and headings at page 1, before line 4:

CROSS-REFERENCE TO RELATED APPLICATIONS

B3 This application is a divisional of U.S. Patent Application Serial No. 08/737,192, filed March 28, 1997, now U.S. Patent No. 6,052,426, which is a continuation of PCT Application No. PCT/FR95/00634, filed May 16, 1995, and claims priority to French Patent Application No. 94 05987, filed May 17, 1994.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

Please insert the following heading at page 1, before line 9:

B4 DISCUSSION OF THE BACKGROUND

Please amend the paragraph at page 1, line 35 through page 2, line 6, as follows:

B5 In a flat television or computer screen, the fact that the number of pixels is very large, that the spacing of the grid of these pixels is very small, thus limiting the space available in which to place the control circuit, and that a large number of selection lines and data lines are

~~[sic]~~ required, compels the use of the smallest and simplest possible control circuits so as to achieve a high degree of manufacturing efficiency. It may moreover be advantageous to use semiconductor devices as pixel switching devices, with the same conductivity type throughout the display.

Please amend the paragraph at page 2, lines 7-28, as follows:

Control of these semiconductor devices can be undertaken by lines addressed by one or more shift registers. A register structure such as that represented in Figure 1 provides a partial response to the requirements stated in the previous paragraph. A stage 11 of a register contains six transistors Tp, Td, Ts, Tr, Tl and Tz, and is fed with two clock signals Φ1 and [[Φ3]] Φ2 at 14 and 15, as well as with two positive sources Vdd and one (relatively) negative source Vss. The operation of a shift register made up of such stages is described in detail in International Patent Application WO 92/15992 filed by Thomson LCD. This operation relies on the fact that the gate of the transistor Tl which controls the output 13 of the stage of the register is left floating, and that its potential therefore follows those of the clock and of the output through a capacitive effect. This is the "~~Bootstrap [sic]~~ bootstrap" effect. This allows, at the desired moment, complete charging of the output 13 to the highest potential of the clock Φ1. The transistor Tp allows the gate of the transistor Tl to be precharged and allows the transistor Td to discharge this gate.

Please insert the following heading at page 3, before line 26:

BRIEF SUMMARY OF THE INVENTION

Please amend the paragraph at page 4, lines 16-19, as follows:

· to the output associated with the stage across a second capacitance, the [[said]] output being connected to ~~earth~~ ground across a third semiconductor device controlled by a second node,

Please amend the paragraph at page ~~4~~, lines ~~20-21~~, as follows:

· and to ~~earth~~ ground across a fourth semiconductor device controlled by the second node, this second node being connected moreover:

Please amend the paragraph at page ~~4~~, lines ~~25-26~~, as follows:

· to ~~earth~~ ground across a fifth semiconductor device controlled by the output of the preceding stage,

Please amend the paragraph at page 4, lines ~~31-32~~, as follows:

· and to that terminal of the third semiconductor device connected to ~~earth~~ ground[[,]] by a capacitance.

Please amend the paragraph at page ~~5~~, lines ~~2-5~~, as follows:

· to the output associated with the stage across a second capacitance, the [[said]] output being connected to ~~earth~~ ground across a fourth semiconductor device controlled by a second node,

Please amend the paragraph at page ~~5~~, lines ~~22-28~~, as follows:

According to important characteristics of the invention, the first and second clock signals are complementary, the first capacitance has a value equivalent to the value of the

B13 Cont. stray capacitance of the semiconductor output device, and the second capacitance has a value substantially greater than that of the stray capacitance of the semiconductor output device.

Please amend the paragraph at page 5, lines 29-31, as follows:

B14 The present invention also extends to all types of flat active-matrix ~~screen~~ screens which use peripheral or integrated control circuits.

Please insert the following heading at page 6, between lines 13 and 14:

B15 BRIEF DESCRIPTION OF THE DRAWINGS

Please insert the following heading at page 7, between lines 1 and 2:

B16 DESCRIPTION OF THE PREFERRED EMBODIMENTS

Please amend the paragraph at page 7, lines 31-34, as follows:

B17 The node D is connected to the source of the transistor Tl, to the node G via a capacitance Cb, and to the line J to be selected, whose load ~~which~~ is symbolized electrically by a capacitance Cl.

Please amend the paragraph at page 8, lines 6-15, as follows:

B18 Thus, these stray effects - consequences of the bootstrap effect - are counterbalanced by virtue of the linking of the clock Φ2, the complement of the clock Φ1, with the gate of the transistor Tl via the capacitance C2, with a value [[Ct]] equivalent to that of Cp. Since the two clocks are exactly complementary they do not give rise to any stray voltage at the node G and hence at the gate of the transistor T_l. An equivalent circuit contains a capacitance ~~C1=2xCt~~ Cl=2xC2 between the node G and ~~earth~~ ground 32.

Please amend the paragraph at page 8, lines 16-22, as follows:

Since such a structure diminishes the bootstrap effect, it is necessary to add a bootstrap capacitance Cb between the source node D and the gate node G so that the voltage of the gate follows a fraction Cb/(Cb+2×Cp) of the variations of the source voltage. Thus, in order to attain a bootstrap ratio of 60%, it suffices for Cb to be three times the value of [[Ct]] C2.

Please amend the paragraph at page 9, lines 30-36, as follows:

The transistor Td should not be overdimensioned, so that the transistor Tl remains on for long enough for the output J to return completely to zero. As the source of the transistor Tl is slightly negatively biased, the node G attains a negative voltage when idle, so that the transistor Tl is ~~more definitely~~ blocked to a relative greater degree than in the prior art of Figure 1.

Please amend the paragraph at page 10, lines 8-22, as follows:

According to an important characteristic of the invention, a transistor Tz for resetting the source of the output transistor Tl to zero connects the bootstrap capacitance Cb to ~~earth~~ ground at 33. The gate of this transistor [[47]] Tz is controlled by the node Z, connected on one side to the gate of the discharge transistor Td and on the other hand to the next line J+1 via two clamping transistors (gate connected to the source) Th and Tg mounted in parallel head-to-tail, the drains of the two transistors being connected to the sources and the gates being controlled by the sources. That is to say that one, the transistor Tg, is controlled by the node Z and the other, the transistor Th by the line of the next stage J+1. A capacitance Cg is connected on one side to the node Z and on the other to ~~earth~~ ground at 33.

Please amend the paragraph at page 10, lines 23-29, as follows:

B22 Moreover, the transistor Td connects the node G to ~~earth~~ ground, and its gate is controlled by the node Z. The latter is connected to ~~earth~~ ground across a transistor Tr whose gate is controlled by the node H, that is to say by the output J-1 of the preceding stage. The node Z is furthermore connected to the node H by a capacitance Cc.

Please amend the paragraph at page 10, line 30 through page 11, line 12, as follows:

The operation of this circuit is essentially the same, in respect of the common parts, as that of the circuit of Figures 2 and 3a to 3f of the previous embodiment of the invention. The enhancement as compared with the latter embodiment is that, when idle, the gates of the B23 transistors Tz and Td, that is to say the node Z, are maintained at the level of their threshold voltage. These transistors are then sufficiently passing to maintain the nodes G and D at the low potential. In this case, the transistor Tp no longer serves under these conditions to bring the potential of the outputs to the low point. By virtue of the two transistors Th and Tg by which it is connected to the line 30 (the line of the following stage), the potential of the node Z is maintained at the threshold voltage of the transistors Td and Tz. The node Z will therefore follow the voltage variations of J+1 with a voltage lag equivalent to the threshold voltage of the transistors. Thus, when J+1 rises, the node Z reaches the positive voltage minus the threshold voltage, and the potentials of the nodes G and D are brought to zero. The transistors Td and Tz are then ~~being~~ fully on.

Please amend the paragraph at page 12, lines 15-23, as follows:

B24 When the stage 45 is selected, that is to say in order ~~than~~ that the line J, the output of stage 45, be suitably charged (Figure 5e), the node Z must remain at the level of the threshold

voltage of the transistors Td and Tz. But, at this instant, J+1 is at the low level of the clocks (Figure 5f). Bearing in mind the existence of the transistors Th and Tg, the low level of the clocks must therefore not exceed twice the threshold of the transistors.

Please amend the paragraph at page 13, line 31 through page 14, line 12, as follows:

The reset signal controlling the gate of the transistor Tz is a signal consisting of a short pulse of width Tl lagging in phase with respect to the clock signals Φ1 and Φ2, and which has a period equal to half that of Φ1 and Φ2, as is illustrated by Figure 8. Moreover, the transistor Td whose gate is controlled by the next line J+1 is activated at its source by a signal V with the same frequency as the reset signal controlling the transistor Tz, and with width T2 at the start of each half-period. This is so as to prevent the transistor Td from discharging the node G too quickly, before the node D, that is to say the line J, has fallen back to the ~~earth~~ ground level. In fact, when V is positive for the duration T2, the transistor Td cannot discharge the point G, so that Tl can bring the potential of line J (node D) to ~~earth~~ ground. Thus, each output is ~~earth~~ grounded at each line addressing time for the short duration Tl. This embodiment of the invention may be termed "medium impedance" (low impedance only during the time for which the reset lasts and high impedance for the remainder of the time).

Please amend the paragraph at page 14, lines 13-26, as follows:

A fifth embodiment of the invention represented in Figure 9 consists in controlling the gate of the transistor Tz with a reset signal and controlling the gate of the transistor Td with a clock signal Φa chosen from three clock signals Φa, Φb and Φc. The source of the transistor Td is maintained at a constant negative potential V-. As Figure 10 shows, each of these clocks consists of a short pulse of duration T3 lagging behind the alternating transitions of

Φ1and Φ2, and has a repeat period which is three times that of the reset signal. The three clocks Φa, Φb and Φc are derived from one another through a lag equal to the reset period which corresponds to the line addressing period. This embodiment may be termed "low impedance." [[.]]